Battery Management System

Avnet Design Service
Battery Management System introduction

This system is made up of main board, load board (or cell array) and GUI. When two board are power on, main board will gather the information about Voltage, temperature, current from the load and send to PC. GUI will process the information by simple SOC algorithm and SOH, and then display it. The main used ICs are supplied by ADI and Freescale.
BMS features

- Support 12 cells, current and voltage measure
- GUI support configure the parameters and gather the data from the board
- ±1.6 mV cell voltage accuracy
- VDD operating range: 8 V to 30 V
- Temperature range: −40° C to +105° C
- 12-bit ADC, 1 µs per channel conversion time
- CM range 0.5 V to 27.5 V
- VDD operating range: 8 V to 30 V
Battery Management System
Main board Diagram

+HV

Cell Pack (GP)

Cell Pack (GP)

AD7280A

Voltage
Temperature
Balance

Voltage
Temperature
Balance

Isolators ADuM 1401

Isolators ADuM 5401

MCU 9S12P64 J0MLHS

RS-232 Interface

Current_Sen

Isolated Sigma-Delta Modulator AD7400A

Amplifiers AD8646

PC
AD7280A Introduction

AD7280A contains all the functions required for general-purpose monitoring of stacked lithium ion batteries as used in hybrid electric vehicles, battery backup applications, and power tools. The part has multiplexed cell voltage and auxiliary ADC measurement channels for up to six cells of battery management.
AD7280A Block Diagram
AD7280A advantage

Register

• 6 Cells & 6 AUX Reads
• 2 Control
• 1 CNVST Control
• 1 Self Test
• 6 Cell Balance
• 4 Alert Threshold (OV, UV, OT & UT)
• Alert Register
• Power Timer
• Read Register
AD7280A advantage

1. High Efficiency
2. Isolation
3. Low Noise
4. Temperature Stability
5. High Flexibility
Daisy chained AD7280As should be on same PCB, shorten daisy chain wires
Recommend SPI frequency < 1MHz
Shield all daisy chain tracks well to reduce EMC/EMI issue.
22pF cap at daisy chain lines, close to termination pin (arrow side).
<=30V zener on power supply line (power supply rating 8V~30V)
Ferrite or 20Ω resistor on VDD line, and VSS line
Route VDD & VSS lines with low impedance and low inductance
Pull-up/down resistor at MASTER & unused SPI / IO pins
Schematics Introduction

- VDRIVE pin controls the voltage at which SPI operates, enabling interface to 3V/5V processor.
- VDRIVE can be supplied by external, or connected to VREG (internal 5V regulator).
- VREG load current = 5mA max for external load, in addition to AVCC, DVCC, VDRIVE consumption.
- Be careful to drive external isolation circuit!
- Voltage on VIN6 pin must >= VDD supply voltage
- To connect less than 6 cells, refer to graphic:
- Regardless of how many cells connected, AD7280A acquire and convert all 6 input channels.
Schematics Introduction

- 6 cell balancing outputs
- Each CB output is used to switch on/off an external FET
- CB output is triggered by writing to cell balance register
- Each CB(n) output is 0V/5V with respect to Vin(n-1)
- A timer can be programmed on each CB output to allow it to switch off automatically after 0 to 36.9min
- CB outputs are switched off when AD7280A power down
- 10kΩ resistor should be put between CB output and FET to protect AD7280A under abnormal cases:
  Improper initial connection sequence between cells and AD7280A; External FET fails or damaged
- External FET also should be protected during initial connection of the cells
MCU and AD7280A

Table 32. 32-Bit Write Cycle

<table>
<thead>
<tr>
<th>Device Address</th>
<th>Register Address</th>
<th>Register Data</th>
<th>Address All Parts</th>
<th>Reserved (Zero-bit)</th>
<th>8-bit CRC</th>
<th>Reserved (Zero-bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D31-D27</td>
<td>D26-D21</td>
<td>D20-D13</td>
<td>D12</td>
<td>D11</td>
<td>D10-D3</td>
<td>D2-D0</td>
</tr>
</tbody>
</table>

Table 33. 32-Bit Read Conversion result Cycle

<table>
<thead>
<tr>
<th>Device Address</th>
<th>Channel Address</th>
<th>Conversion Data</th>
<th>Write Acknowledge</th>
<th>8-bit CRC</th>
<th>Reserved (Zero-bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D31-D27</td>
<td>D26-D23</td>
<td>D22-D11</td>
<td>D10</td>
<td>D9-D2</td>
<td>D1-D0</td>
</tr>
</tbody>
</table>

Table 34. 32-Bit Read Register Data Cycle

<table>
<thead>
<tr>
<th>Device Address</th>
<th>Register Address</th>
<th>Register Data</th>
<th>Zero</th>
<th>Write Acknowledge</th>
<th>8-bit CRC</th>
<th>Reserved (Zero-bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D31-D27</td>
<td>D26-D21</td>
<td>D20-D13</td>
<td>D12-D11</td>
<td>D10</td>
<td>D9-D2</td>
<td>D1-D0</td>
</tr>
</tbody>
</table>

Image of waveform and timing diagram for SPI communication.
## Communication Introduction (2)

### MCU and PC

The command write/read packet format

<table>
<thead>
<tr>
<th>content</th>
<th>STC0</th>
<th>STC1</th>
<th>INS</th>
<th>LEN</th>
<th>DATA</th>
<th>CHKSUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>frame</td>
<td>0xa</td>
<td>0xf5</td>
<td>SPEC</td>
<td>0~64</td>
<td>SPEC</td>
<td></td>
</tr>
</tbody>
</table>

The response packet format

<table>
<thead>
<tr>
<th>content</th>
<th>STC0</th>
<th>STC1</th>
<th>STS</th>
<th>LEN</th>
<th>DATA</th>
<th>CHKSUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>frame</td>
<td>0xa</td>
<td>0xf5</td>
<td>SPEC</td>
<td>0~64</td>
<td>SPEC</td>
<td></td>
</tr>
</tbody>
</table>
Communication Introduction(3)

MCU and PC

- STC0, STC1: head
- INS: command
- LEN: data length
- STS: command status
- DATA: data
- CHKSUM: checksum

<table>
<thead>
<tr>
<th>STS</th>
<th>Content</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Ready/OK</td>
<td>Command executed without ERROR and MCU/PC is waiting for next command</td>
</tr>
<tr>
<td>A2</td>
<td>Data Ready</td>
<td>Data is ready for reading</td>
</tr>
<tr>
<td>A3</td>
<td>Error</td>
<td>Command is error and error reason is shown in DATA field of response packet.</td>
</tr>
</tbody>
</table>
## Communication Introduction(4)

### MCU and PC

<table>
<thead>
<tr>
<th>Code</th>
<th>Command</th>
<th>R/W</th>
<th>length</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xb1</td>
<td>Configure</td>
<td>W</td>
<td>0</td>
<td>Configure the parameter such as OverVOI etc</td>
</tr>
<tr>
<td>0xb6</td>
<td>Read Status</td>
<td>R</td>
<td>4</td>
<td>Read the operation status, V, T, of the slave node</td>
</tr>
</tbody>
</table>
GUI introduction

Display

Configuration

Voltage, current

Remain battery

Fault alarm

Configure COM
Battery Management System
Main Board Photo

- AD7280A
- 2N7002W
- AD8646
- NCV4275
- MC9S12P128
- ADuM1401
- ADuM5401
- AD7400A
Battery Management System
Load board Photo
Avnet support

- Designs can be customized to meet specific requirements
- Demo units, sample boards
- Schematics, BOM, test and troubleshooting documentation
- Training for key engineers
- Supply of components used in the design
- Support for programming the MCU during mass production
- Post-design support

Please contact Keven Chen (13818250911)
Thank You